

- Low  $r_{DS(on)}$  . . . 1.3  $\Omega$  Typ
- Avalanche Energy . . . 75 mJ
- Eight Power DMOS Transistor Outputs of 250-mA Continuous Current
- 1.5-A Pulsed Current Per Output
- Output Clamp Voltage at 45 V
- Enhanced Cascading for Multiple Stages
- All Registers Cleared With Single Input
- Low Power Consumption

## description

The TPIC6596 is a monolithic, high-voltage, high-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

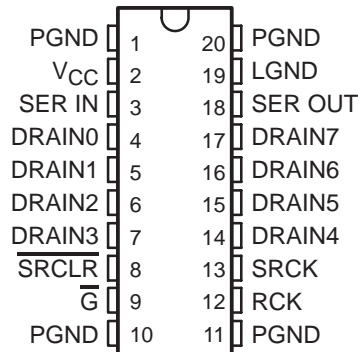
This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK) respectively. The storage register transfers data to the output buffer when shift-register clear (SRCLR) is high. When SRCLR is low, all registers in the device are cleared. When output enable ( $\overline{G}$ ) is held high, all data in the output buffers is held low and all drain outputs are off. When  $\overline{G}$  is held low, data from the storage register is transparent to the output buffers. The serial output (SER OUT) is clocked out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This will provide improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference.

Outputs are low-side, open-drain DMOS transistors with output ratings of 45 V and 250-mA continuous sink current capability. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink current capability.

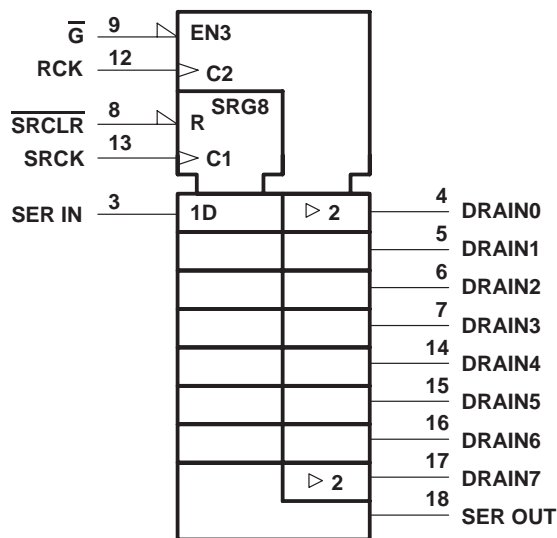
Separate power and logic level ground pins are provided to facilitate maximum system flexibility. Pins 1, 10, 11, and 20 are internally connected, and each pin must be externally connected to the power system ground in order to minimize parasitic inductance. A single-point connection between pin 19, logic ground (LGND), and pins 1, 10, 11, and 20, power grounds (PGND), must be externally made in a manner that reduces crosstalk between the logic and load circuits.

The TPIC6596 is characterized for operation over the operating case temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

**DW OR N PACKAGE  
(TOP VIEW)**



## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

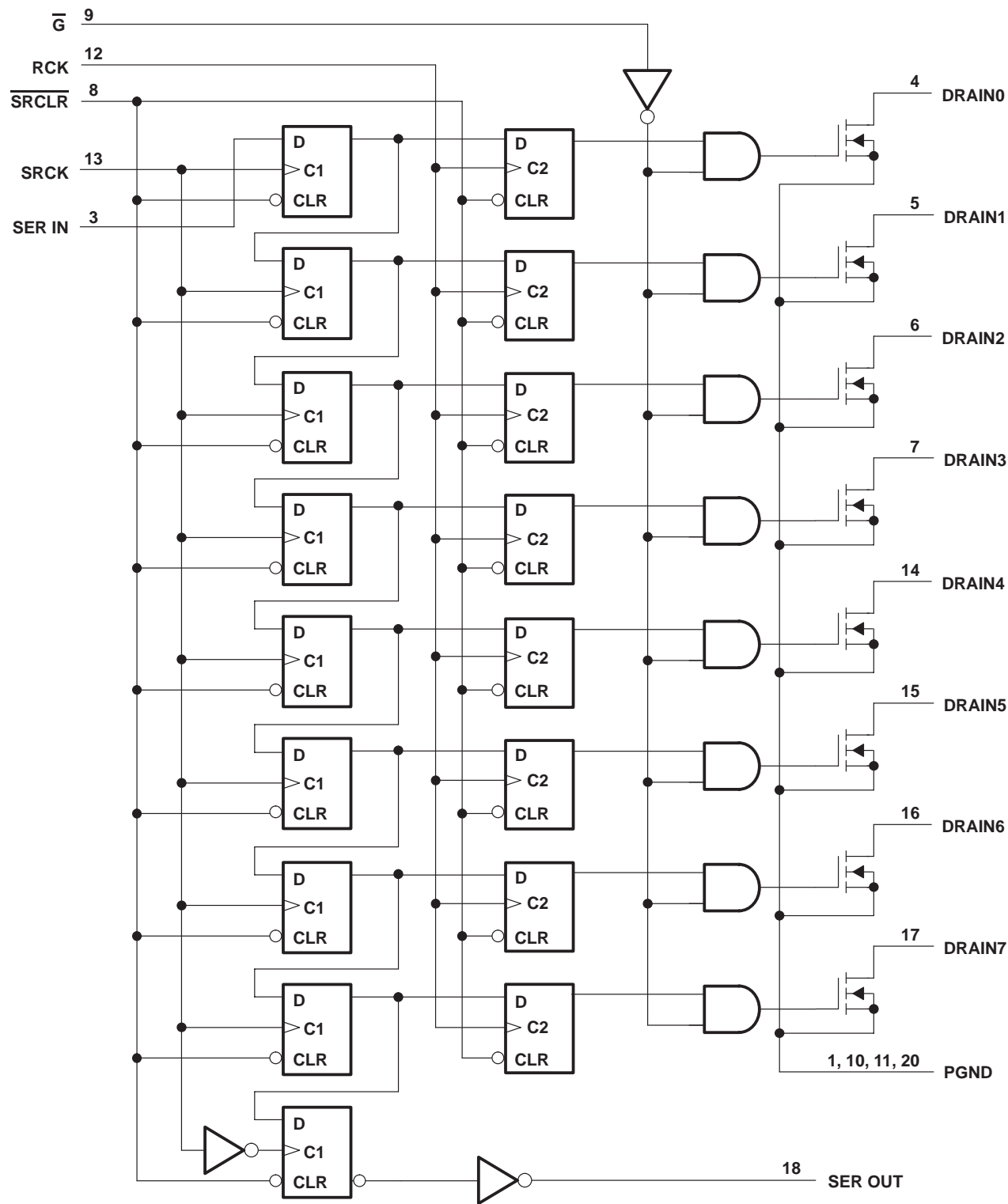
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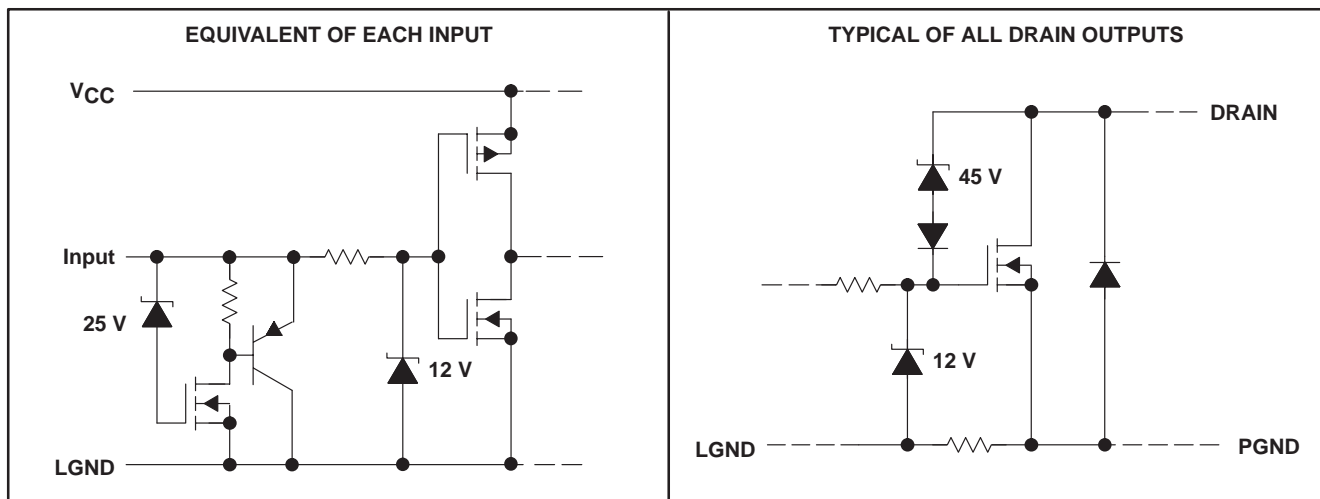
# TPIC6596 POWER LOGIC 8-BIT SHIFT REGISTER

SLIS096A – APRIL 2000 – REVISED MAY 2005

## logic diagram (positive logic)



## schematic of inputs and outputs



## absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)<sup>†</sup>

Logic supply voltage, $V_{CC}$ (see Note 1)	7 V
Logic input voltage range, $V_I$	–0.3 V to 7 V
Power DMOS drain-to-source voltage, $V_{DS}$ (see Note 2)	45 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current	2 A
Pulsed drain current, each output, all outputs on, $I_{Dn}$ , $T_A = 25^\circ\text{C}$ (see Note 3)	750 mA
Continuous drain current, each output, all outputs on, $I_{Dn}$ , $T_A = 25^\circ\text{C}$	250 mA
Peak drain current single output, $I_{DM}$ , $T_A = 25^\circ\text{C}$ (see Note 3)	2 A
Single-pulse avalanche energy, $E_{AS}$ (see Figure 4)	75 mJ
Avalanche current, $I_{AS}$ (see Note 4)	1 A
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, $T_J$	–40°C to 150°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values are with respect to LGND and PGND.
  2. Each power DMOS source is internally connected to PGND.
  3. Pulse duration  $\leq 100 \mu\text{s}$ , duty cycle  $\leq 2\%$
  4. DRAIN supply voltage = 15 V, starting junction temperature ( $T_{JS}$ ) = 25°C,  $L = 100 \text{ mH}$ ,  $I_{AS} = 1 \text{ A}$  (see Figure 4).

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 125^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
N	1150 mW	9.2 mW/°C	230 mW

# TPIC6596

## POWER LOGIC 8-BIT SHIFT REGISTER

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**recommended operating conditions over recommended operating temperature range (unless otherwise noted)**

	MIN	MAX	UNIT
Logic supply voltage, $V_{CC}$	4.5	5.5	V
High-level input voltage, $V_{IH}$	0.85 $V_{CC}$		V
Low-level input voltage, $V_{IL}$		0.15 $V_{CC}$	V
Pulsed drain output current, $T_C = 25^\circ\text{C}$ , $V_{CC} = 5\text{ V}$ (see Notes 3 and 5)	-1.8	1.5	A
Setup time, SER IN high before SRCK $\uparrow$ , $t_{SU}$ (see Figure 2)	10		ns
Hold time, SER IN high after SRCK $\uparrow$ , $t_H$ (see Figure 2)	10		ns
Pulse duration, $t_W$ (see Figure 2)	20		ns
Operating case temperature, $T_C$	-40	125	$^\circ\text{C}$

NOTES: 3. Pulse duration  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 2\%$   
5. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.

**electrical characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_C = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>(BR)DSX</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA		45			V
V <sub>SD</sub>	Source-drain diode forward voltage	I <sub>F</sub> = 250 mA, See Note 3			0.85	1	V
V <sub>OH</sub>	High-level output voltage, SER OUT	I <sub>OH</sub> = −20 mA, V <sub>CC</sub> = 4.5 V		4.4	4.49		V
		I <sub>OH</sub> = −4 mA, V <sub>CC</sub> = 4.5 V		4.1	4.3		
V <sub>OL</sub>	Low-level output voltage, SER OUT	I <sub>OH</sub> = 20 mA, V <sub>CC</sub> = 4.5 V			0.002	0.1	V
		I <sub>OH</sub> = 4 mA, V <sub>CC</sub> = 4.5 V			0.2	0.4	
V <sub>(hys)</sub>	Input hysteresis	V <sub>DS</sub> = 15 V			1.3		V
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub>				1	μA
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0				−1	μA
I <sub>CCL</sub>	Logic supply current	I <sub>O</sub> = 0, All inputs low			15	100	μA
I <sub>CC(FRQ)</sub>	Logic supply current frequency	f <sub>SRCK</sub> = 5 MHz, I <sub>O</sub> = 0, C <sub>L</sub> = 30 pF, See Figures 1, 2, and 6			0.6	5	mA
I <sub>N</sub>	Nominal current	V <sub>DS(on)</sub> = 0.5 V, I <sub>N</sub> = I <sub>D</sub> , T <sub>C</sub> = 85°C	See Notes 5, 6, and 7		250		mA
I <sub>DSX</sub>	Off-state drain current	V <sub>DS</sub> = 40 V			0.05	1	μA
		V <sub>DS</sub> = 40 V, T <sub>C</sub> = 125°C			0.15	5	
r <sub>DS(on)</sub>	Static drain-source on-state resistance	I <sub>D</sub> = 250 mA, V <sub>CC</sub> = 4.5 V	See Notes 5 and 6 and Figures 9 and 10		1.3	2	Ω
		I <sub>D</sub> = 250 mA, T <sub>C</sub> = 125°C, V <sub>CC</sub> = 4.5 V			2	3.2	
		I <sub>D</sub> = 500 mA, V <sub>CC</sub> = 4.5 V			1.3	2	

NOTES: 3. Pulse duration  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 2\%$   
5. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.  
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.  
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of  $0.5\text{ V}$  at  $T_C = 85^\circ\text{C}$ .

**switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_C = 25^\circ\text{C}$**

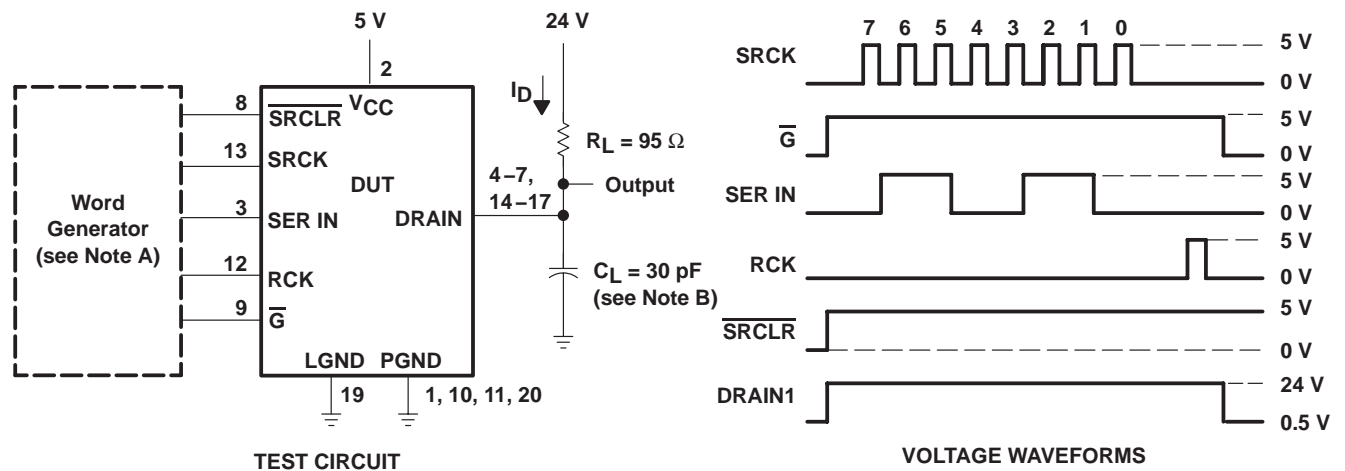
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low-to-high-level output from $\overline{G}$	$C_L = 30\text{ pF}$ , $I_D = 250\text{ mA}$ , See Figures 1, 2, and 11		650		ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from $\overline{G}$			200		ns
$t_r$ Rise time, drain output			230		ns
$t_f$ Fall time, drain output			170		ns
$t_{pd}$ Propagation delay time, $SRCK \downarrow$ to $SER\ OUT$	$C_L = 30\text{ pF}$ , $I_D = 250\text{ mA}$ , See Figure 2		50		ns
$f_{(SRCK)}$ Serial clock frequency	$C_L = 30\text{ pF}$ , $I_D = 250\text{ mA}$ , See Note 8			5	MHz
$t_a$ Reverse-recovery-current rise time	$I_F = 250\text{ mA}$ , $di/dt = 20\text{ A}/\mu\text{s}$ , See Notes 5 and 6 and Figure 3		100		ns
$t_{rr}$ Reverse-recovery time			300		

- NOTES: 5. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.  
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.  
8. This is the maximum serial clock frequency assuming cascaded operation where serial data is passed from one stage to a second stage. The clock period allows  $SRCK \rightarrow SER\ OUT$  propagation delay and setup time plus some timing margin.

**thermal resistance**

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$ Thermal resistance, junction-to-ambient	DW package		111	$^\circ\text{C}/\text{W}$
	N package		108	

**PARAMETER MEASUREMENT INFORMATION**

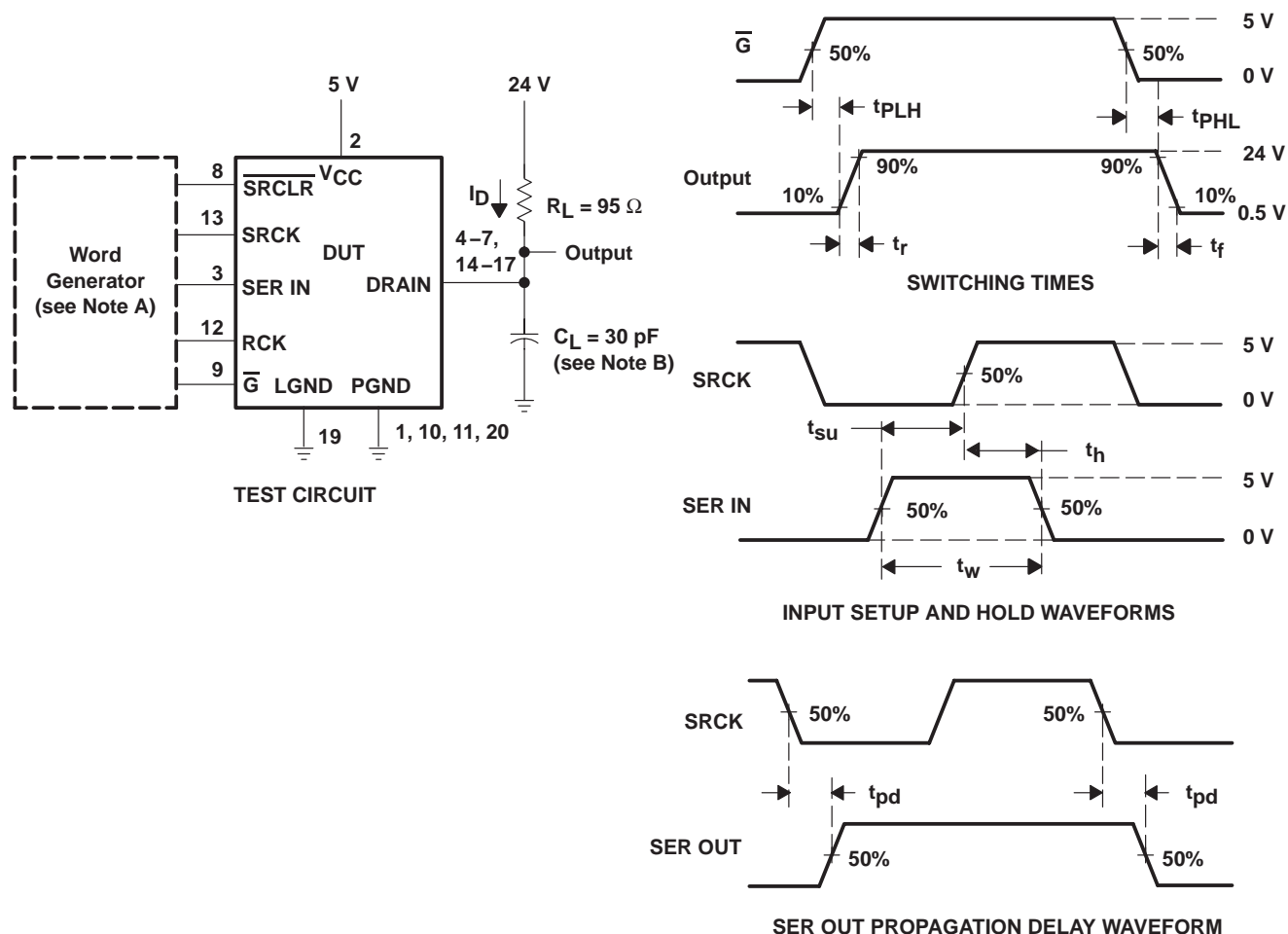


**Figure 1. Resistive Load Operation**

# TPIC6596 POWER LOGIC 8-BIT SHIFT REGISTER

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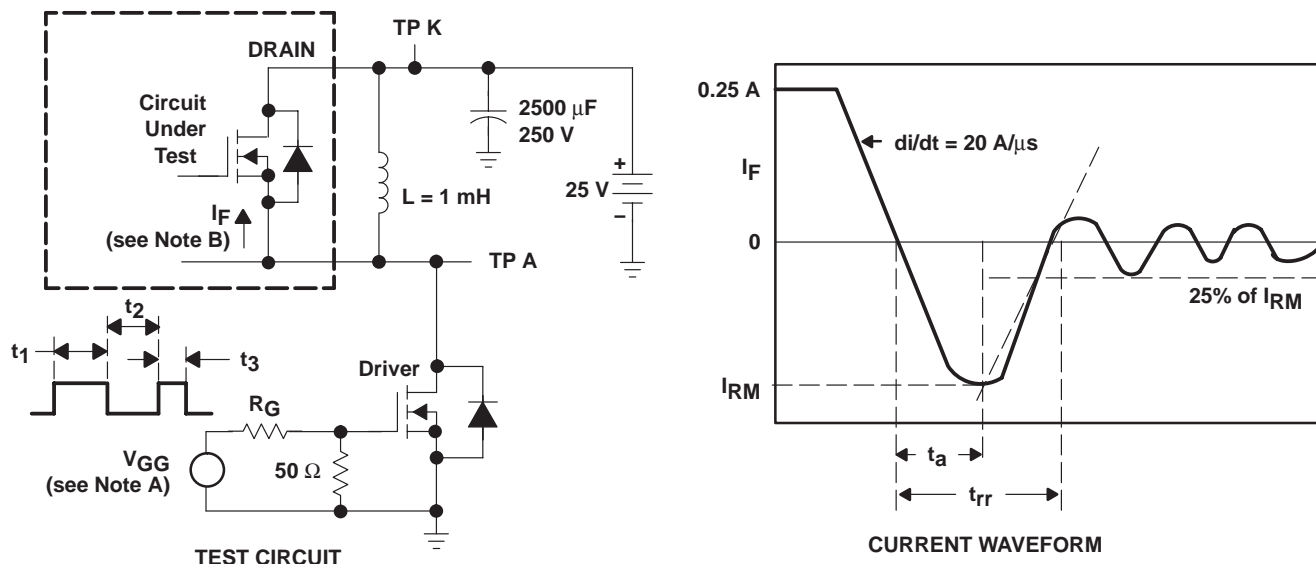
## PARAMETER MEASUREMENT INFORMATION



**Figure 2. Test Circuit, Switching Times, and Voltage Waveforms**

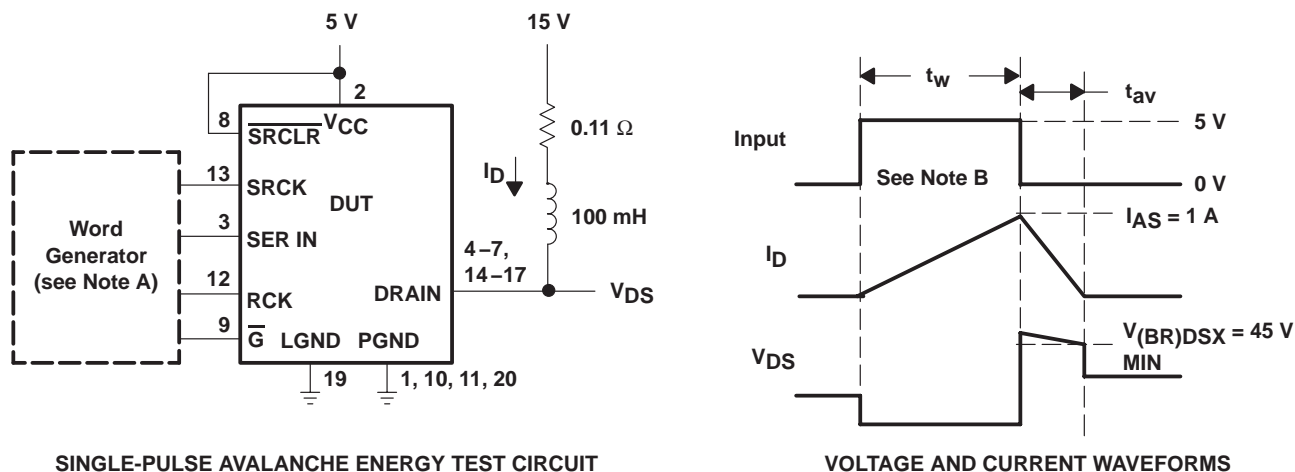
- NOTES: A. Outputs DRAIN 1, 2, 5, and 6 low (PGND), all other DRAIN outputs are at 24 V. The word generator has the following characteristics:  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ ,  $t_w = 300 \text{ ns}$ , pulsed repetition rate (PRR) = 5 kHz,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes probe and jig capacitance.

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The  $V_{GG}$  amplitude and  $R_G$  are adjusted for  $di/dt = 20 \text{ A}/\mu\text{s}$ . A  $V_{GG}$  double-pulse train is used to set  $I_F = 0.25 \text{ A}$ , where  $t_1 = 10 \mu\text{s}$ ,  $t_2 = 7 \mu\text{s}$ , and  $t_3 = 3 \mu\text{s}$ .  
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



- NOTES: A. The word generator has the following characteristics:  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ ,  $Z_O = 50 \Omega$ .  
B. Input pulse duration,  $t_w$ , is increased until peak current  $I_{AS} = 1 \text{ A}$ .  
Energy test level is defined as  $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 75 \text{ mJ}$ , where  $t_{av}$  = avalanche time.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

# TPIC6596

## POWER LOGIC 8-BIT SHIFT REGISTER

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### TYPICAL CHARACTERISTICS

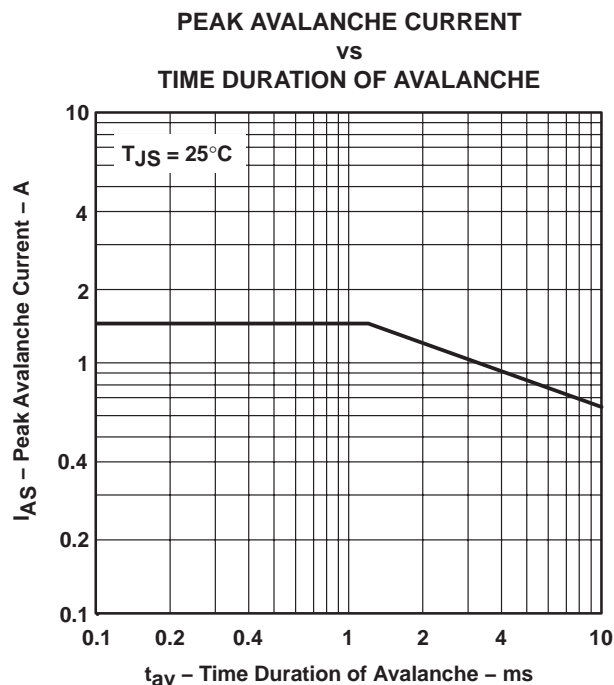


Figure 5

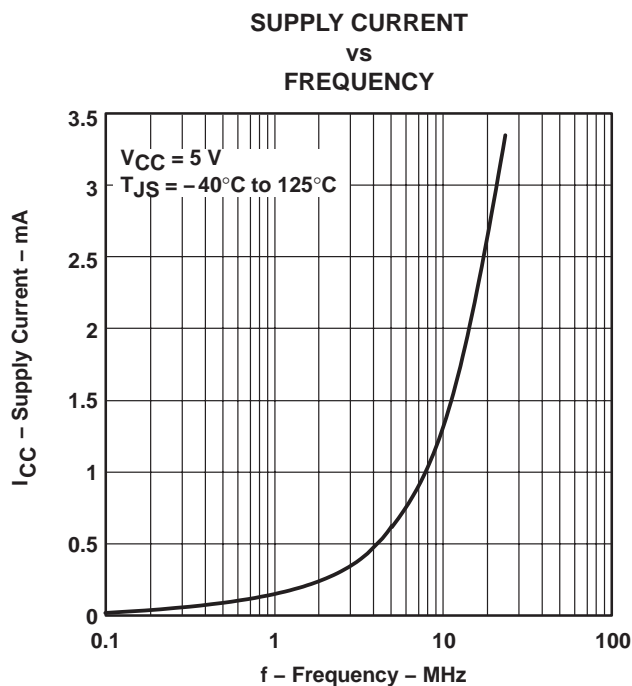


Figure 6

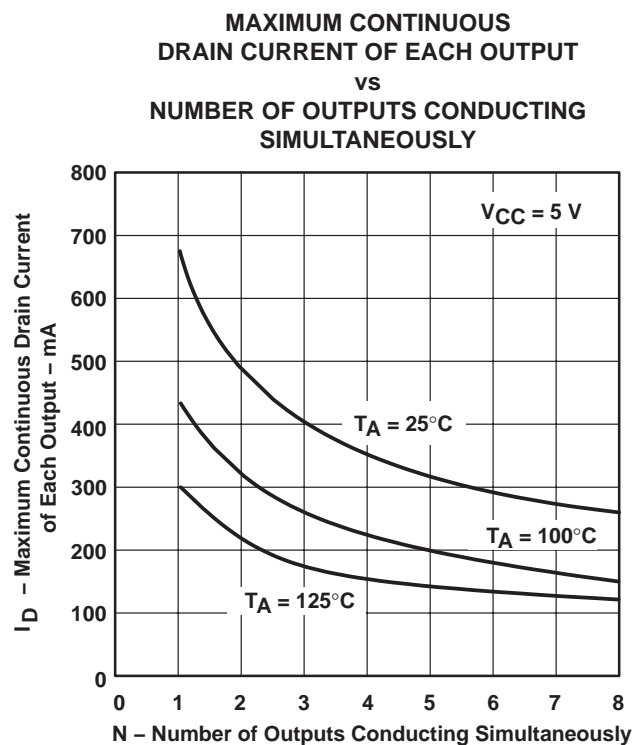


Figure 7

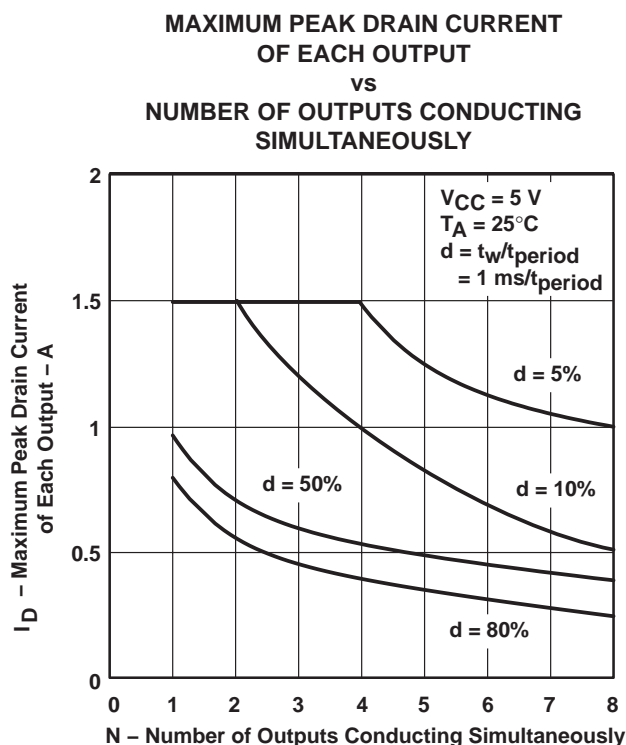


Figure 8



## TYPICAL CHARACTERISTICS

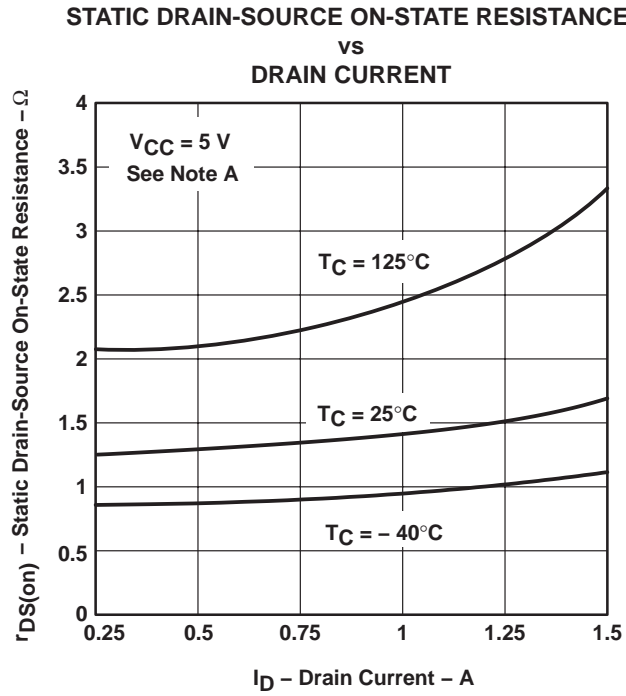


Figure 9

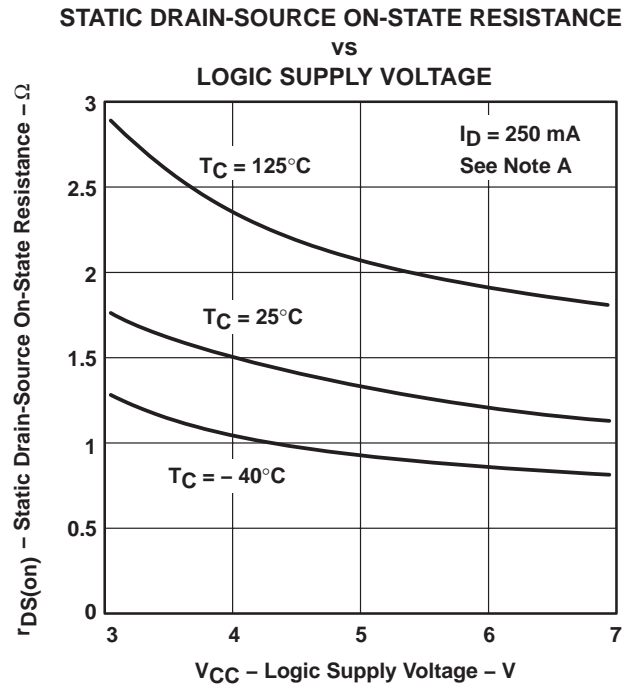


Figure 10

TPIC6596  
POWER LOGIC 8-BIT SHIFT REGISTER

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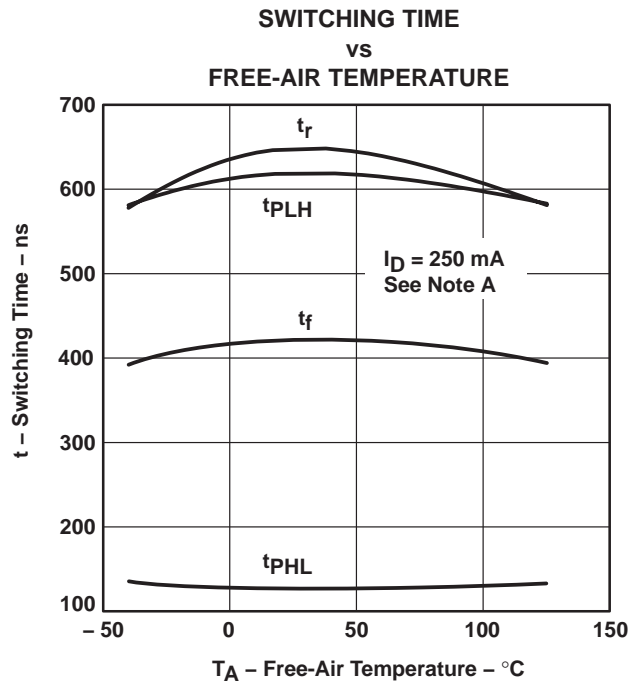


Figure 11

NOTE A: Technique should limit  $T_J - T_C$  to 10°C maximum.

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
5/18/05	A	5	Figure 1	Changed <u>SRCLR</u> timing diagram
4/2000	*			Original reversion

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPIC6596DW	ACTIVE	SOIC	DW	20	25	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPIC6596DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPIC6596DWR	ACTIVE	SOIC	DW	20	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPIC6596DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPIC6596N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DW (R-PDSO-G20)

## PLASTIC SMALL-OUTLINE PACKAGE



4040000-4/F 06/2004

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
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